espagement - Document Dionography and Avostract

Silicon wafer especially SOI wafer production	
Patent Number:	□ <u>DE19753494</u>
Publication date:	1998-10-01
Inventor(s):	YAMAMOTO HIDEKAZU (JP)
Applicant(s):	MITSUBISHI ELECTRIC CORP (JP)
Requested Patent:	☐ <u>FR2761526</u>
Application Number:	DE19971053494 19971202
Priority Number(s):	JP19970080939 19970331
IPC Classification:	H01L21/20; H01L21/324
EC Classification:	H01L21/762D8B
Equivalents:	☐ <u>FR2762136</u> , ☐ <u>JP10275905</u> , TW409418
Abstract	
A silicon wafer (6) production process involves (a) implanting hydrogen ions through a silicon oxide layer-coated silicon wafer surface to form a hydrogen-implanted layer (4); (b) bonding a substrate (5) to the wafer surface; (c) heating the wafer (1) to break off its surface at the hydrogen-implanted layer (4); and (d) heating the wafer portion (6), bonded to the substrate (5), in a hydrogen atmosphere to smooth the exposed broken surface of the wafer (6). Also claimed is a similar silicon wafer (6) production process, in which step (d) is replaced by (d') epitaxial silicon growth on the broken surface to form a new smooth surface. Preferably, step (d) is carried out by annealing at 1050-1350 deg C, plasma heating in a hydrogen atmosphere or rapid thermal annealing and step (d') is carried out by epitaxial growth in trichlorosilane, dichlorosilane, monochlorosilane or monosilane at \-800 deg C. Further claimed is a silicon wafer produced by one of the above processes.	
Data supplied from the esp@cenet database - I2	